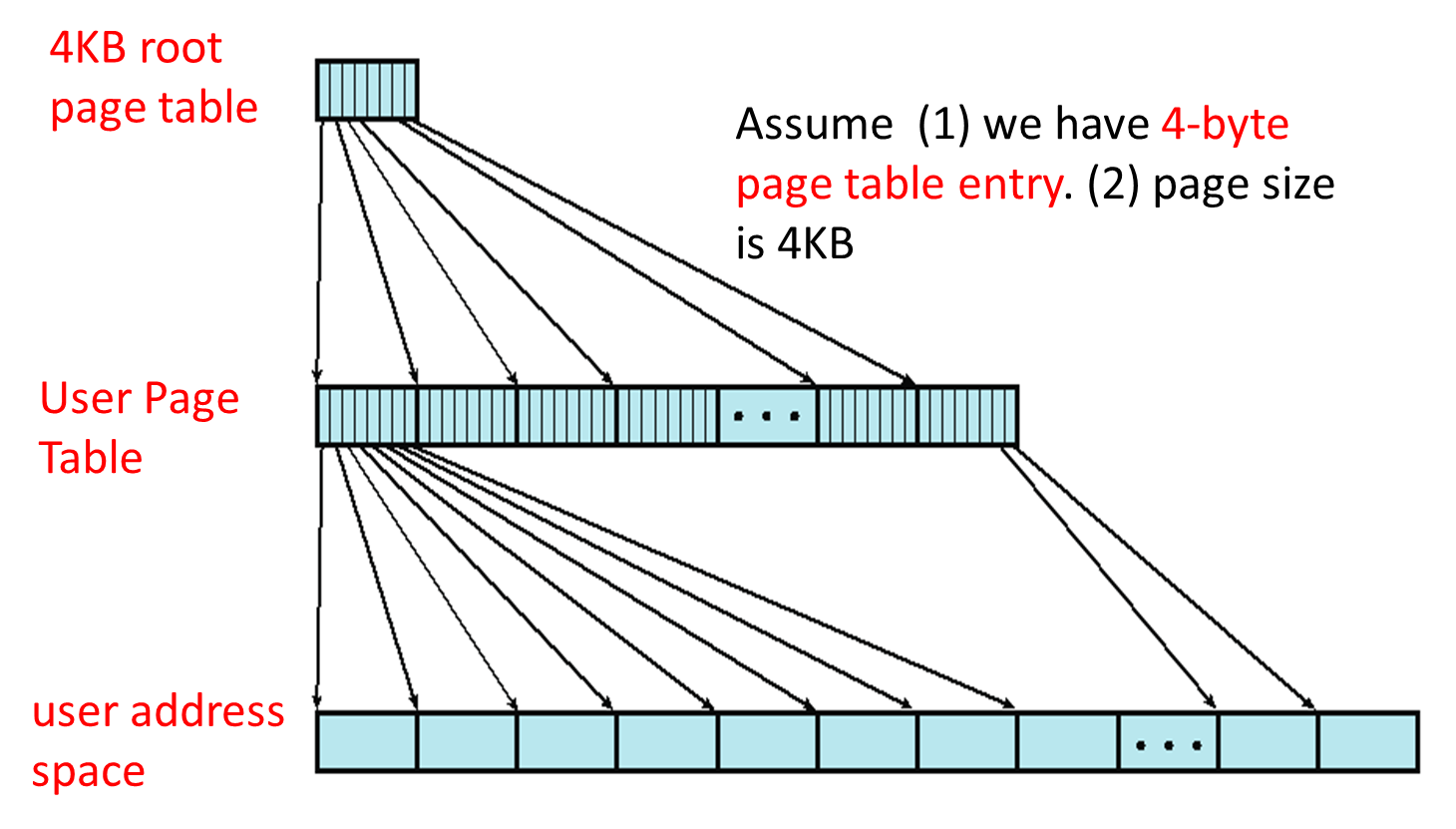
# COMP3500: Translation Look-aside Buffers (TLB)

**Exercise 1 (Plickers):** How many memory accesses are there when a word is accessed from the physical memory? A. 0 B. 1 C. 2 D. 3

**Exercise 2 (Plickers):** We assume each page table entry is 4 bytes, the page size is 4 KB.



Given a 4KB root page table, please answer the following three questions:

(2.1) How many root page table entries?

A. 512; B. 1024; C. 2048; D. 4096

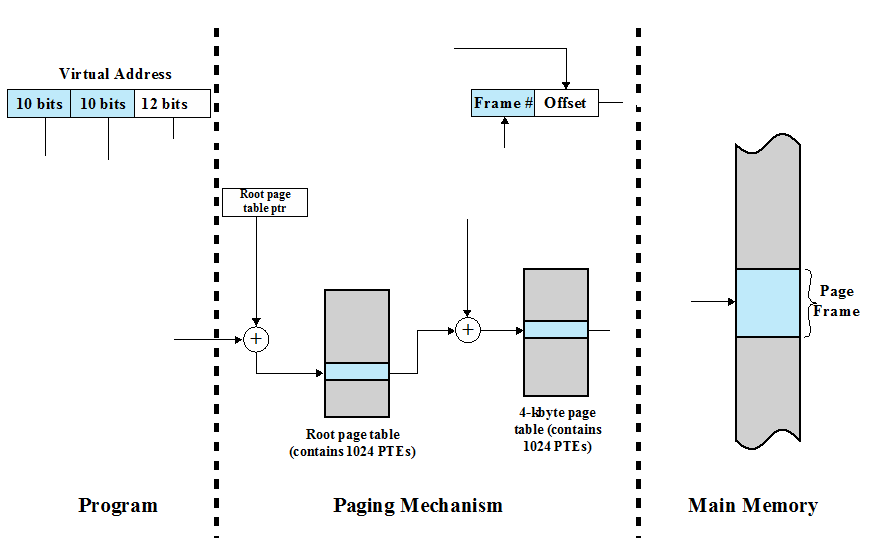
(2.2) How many user page table entries?

A. 1K; B. 512K; C. 1M; D. 4M

(2.3) How large is the user address space?

A. 512MB; B. 1GB; C. 2GB; D. 4GB

**Exercise 3:** How does the address translation work in the two-level paging system?



**Exercise 4 (Plickers):** Suppose you design a two-level page translation scheme where page size is 16MB and page table entry size is 16 bytes. What is the format of a 64-bit virtual address?

1. | 20 bits | 20 bits | 24 bits |
2. | 20 bits | 24 bits | 20 bits |
3. | 24 bits | 20 bits | 20 bits |
4. | 16 bits | 24 bits | 24 bits |

**Exercise 5 (Wheeldecide):** (1)Toload an instruction or data from main memory, how many memory accesses are required in the paging scheme? (2) How can you reduce the number of memory access?

**Exercise 6 (Plickers):** Consider a single-level paging scheme with no data cache. The TLB has 32 entries. The TLB access time is 10 ns; memory access time is 200ns.

* 1. How long does it take to access data in memory if there is a TLB hit?

A. 10 ns

B. 200 ns

C. 210 ns

D. 410 ns

* 1. How long does it take to access data in memory if there is a TLB miss?

A. 200 ns

B. 210 ns

C. 400 ns

D. 410 ns

6.3What is the effective memory-access time if we have a TLB hit ratio of 80%?

A. 210 ns

B. 250 ns

C. 370 ns

D. 410 ns

6.4 What is the minimal hit ratio that guarantees the effective access time of at most 220ns?

A. 85%

B. 90%

C. 95%

D. 98%